IN THE CLAIMS

1. (Previously Amended) A Flash memory device comprising:

a control circuit;

a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each erase block of the plurality of erase blocks contains 128 sectors, and each sector contains a user data section of 512 bytes;

an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field, where the 6 byte erase block management data fields of the first six sectors contain a plurality of differing erase block management data structures; and

a plurality of RAM control registers.

2. (Original) The Flash memory device of claim 1, wherein a first 3 bytes of the 6 byte erase block management data field contain an erase block management data and a second 3 bytes of the 6 byte erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes.

3. (Original) The Flash memory device of claim 1, wherein the first six sectors of each erase block of the plurality of erase blocks are arranged into 3 groups of 2 sector pairs, wherein both sectors of each 2 sector pair contains a complete copy of a erase block management data stored in the 2 sector pair.

4. (Previously Amended) A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further arranged into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and

an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks.

5. (Previously Amended) The Flash memory device of claim 4, wherein the control data sections of the subset of sectors contain a plurality of differing erase block management data fields.

6. (Original) The Flash memory device of claim 4, wherein the erase block management data structure is configured in a fault tolerant data structure.

7. (Original) The Flash memory device of claim 6, wherein the fault tolerant data structure is an erase block management data field and a 1s complement copy of the erase block management data field.

8. (Original) The Flash memory device of claim 6, wherein the fault tolerant data structure is a copy in a second sector of the erase block of an erase block management data field contained in a first sector of the erase block.

9. (Previously Amended) A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells divided into a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and

an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks.

10. (Previously Amended) The Flash memory device of claim 9, wherein the control data section of each sector of the first set of sectors has an erase block management data field.

11. (Previously Amended) The Flash memory device of claim 10, wherein the erase block management data fields of the first set of sectors contain a plurality of differing the erase block management data.

12. (Previously Amended) The Flash memory device of claim 10, wherein the erase block management data field is a six byte data field.

13. (Cancelled)

14. (Previously Amended) The Flash memory device of claim 9, wherein the first set of sectors of the plurality of sectors comprises a first six sectors of each erase block of the plurality of erase blocks.

15. (Previously Amended) A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and

an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks, wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block.

16. (Original) The Flash memory device of claim 15, wherein the erase block state is one of "erased", "invalid", "partially filled", or "fully valid".

17. (Original) The Flash memory device of claim 16, wherein the erase block state is allowed to transition directly from the "partially filled" state to the "invalid" state.

18. (Original) The Flash memory device of claim 15, wherein each erase block of the plurality of erase blocks contains a contiguous range of logical sector addresses.

19. (Original) The Flash memory device of claim 15, wherein each erase block of the plurality of erase blocks contains a single logical sector address that is repeated within the erase block.

20. (Previously Amended) A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section;

a control circuit; and

an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks.

21. (Original) The Flash memory device of claim 20, wherein the control circuit stores equivalents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure.

22. (Original) The Flash memory device of claim 20, wherein the control circuit maps a logical address to a physical address of the plurality of erase blocks.

23. (Original) The Flash memory device of claim 20, wherein the control circuit manages a state of each erase block and erase block management data structure of the plurality of erase blocks.

24. (Original) The Flash memory device of claim 23, wherein the erase block management data structure of each individual erase block of the plurality of erase blocks contains erase block management data for the individual erase block.

25. (Original) The Flash memory device of claim 23, wherein each erase block and erase block management data structure of the plurality of erase blocks is written with an updated user data and an updated erase block management data with a single erase block write operation.

26. (Previously Amended) A system comprising:

a host coupled to a Flash memory device, wherein the Flash memory device comprises,

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further

divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and

an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks.

27. (Original) The system of claim 26, wherein the Flash memory device appears to the host as a rewriteable storage device.

28. (Original) The system of claim 26, wherein the host is a processor.

29. (Original) The system of claim 26, wherein the host is a computer system.

30. (Original) The system of claim 26, wherein an interface to the Flash memory device is compatible with a mass storage device.

31. (Original) The system of claim 26, wherein an interface to the Flash memory device is a PCMCIA-ATA compatible interface.

32. (Previously Amended) A method of making a Flash memory device comprising:

forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section; and

forming an erase block management data structure in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks.

33. (Previously Amended) A method of operating a Flash memory device comprising:

storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors.

34. (Previously Amended) The method of claim 33, wherein storing the erase block management data structure further comprises storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors.

35. (Previously Amended) The method of claim 34, wherein storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors further comprises storing an erase block management data value in a control data section of the subset of sectors.

36. (Previously Amended) The method of claim 34, wherein storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors further comprises storing an erase block management data value in a 6 byte data field of each control data section of the subset of sectors.

37. (Previously Amended) The method of claim 33, wherein storing the erase block management data structure further comprises storing a plurality of differing erase block management data in the control data sections of the subset of sectors of each erase block .

38. (Previously Amended) The method of claim 33, wherein storing the erase block management data structure in a subset of the plurality of sectors of each erase block further comprises storing the erase block management data structure in control data sections of an initial 6 sectors of the erase block.

39. (Previously Amended) A method of operating a Flash memory device comprising:
storing a fault tolerant erase block management data structure in a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors.

40. (Previously Amended) The method of claim 39, wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a component of the erase block management data structure in a first erase block management data field of a first control data section and a 1s complement copy of the component of the erase block management data structure in a second erase block management data field of a second control data section.

41. (Previously Amended) The method of claim 39, wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a copy of an erase block management data field contained in a first control data section of the erase block in a second control data section of the erase block.

42. (Previously Amended) A method of operating a Flash memory device comprising:

placing an erase block management data structure in a control data section of a subset of sectors of a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array; and

recording an erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks.

43. (Previously Amended) The method of claim 42, wherein recording the erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks further comprises recording an erase block identifier that identifies erase block format and content in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks.

44. (Original) The method of claim 43, wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a contiguous range of logical sector addresses.

45. (Original) The method of claim 43, wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a single logical sector address that is repeated within the erase block.

46. (Original) The method of claim 42, wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state as one of "erased", "invalid", "partially filled", or "fully valid".

47. (Original) The method of claim 46, wherein recording the erase block state further comprises allowing the erase block state to transition directly from "partially filled" to "invalid".

48. (Previously Amended) The method of claim 42, wherein recording the erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks further comprises recording the erase block state with an erase block operation that writes both a user data and the erase block management data in a single write operation.

49. (Original) The method of claim 42, further comprising storing the contents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure.

50. (Previously Amended) A method of operating a Flash memory device comprising:
placing an erase block management data structure in a control data section of a subset of sectors of a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array; and
mapping a logical address to a physical erase block and a sector address of the plurality of erase blocks.

51. (Original) The method of claim 50, wherein mapping the logical address to the physical erase block and sector address of the plurality of erase blocks further comprises managing a state of each erase block and erase block management data structure.